CLAIMS filed in response to the first written opinion

1. A method for determining a phase error in response to a first signal and a second signal, said method comprising the steps of:

generating a first reoccurring trigger event in response to the first signal,

generating a second reoccurring trigger event in response to the second signal,

incrementing a first phase value by a first predetermined increment value when the first trigger event occurs to obtain a first accumulated phase value represented by a binary number,

incrementing a second phase value by a second predetermined increment value when the second trigger event occurs to obtain a second accumulated phase value represented by a binary number, and

calculating or determining said phase error based on obtained first and second accumulated phase values, said phase error being represented by a binary number or one or more analogue signals,

said method further comprising the steps of

resetting the most significant bit of the first accumulated phase value and the most significant bit of the second accumulated phase value when the most significant bit of both said first accumulated phase value and said second accumulated phase value are simultaneously 1.

2. A method according to claim 1, wherein the phase error is represented by one or more an analogue signals.

3. A method according to claim 2, said method further comprising the steps of:

performing a first logic bit by bit AND operation of the first accumulated phase value and the inverted second accumulated phase value, and generating a first analogue representation of said first logic bit by bit AND operation, and

performing a second logic bit by bit AND operation of the second accumulated phase value and the inverted first accumulated phase value, and generating a second analogue representation of said second logic bit by bit AND operation.

4. A method according to claim 3, wherein the calculation of the phase error comprises generating one or more analogue phase error signal based on the sec-

ond analogue representation of the second logic bit by bit AND operation and the first analogue representation of the first logic bit by bit AND operation.

5. A method according to claim 4, wherein the calculation of the phase error comprises performing an analogue subtraction of the second analogue representation from the first analogue representation.

6. A method according to any one of the claims 1-5, wherein two equal bits are reset whenever these bits are 1 at the same time.

7. A method according to any one of the claims 1-6, said method comprising the step of frequency dividing the first signal and/or the second signal, whereby the generation of the first and/or second reoccurring trigger event is performed in response to the frequency divided first and/or second signal, respectively.

8. A phase-locked loop comprising:

a voltage controlled oscillator for generating an output signal and having a frequency control input for controlling the frequency of the output signal, and

a phase comparator for deriving a control signal from a phase error detected in response to the received output signal and a reference signal, said control signal being coupled to the frequency control input of said voltage controlled oscillator, wherein the phase comparator includes:

a first accumulator adapted to add a first predefined phase step value to a first accumulated phase value in response to a reoccurring event in the reference signal,

a second accumulator adapted to add a second predefined phase step value to a second accumulated phase value in response to a reoccurring event in the received output signal, and

means or arithmetic means for determining the phase error from the obtained first and second accumulated phase values,

said phase comparator further including a first reset means for the most significant bit of the first accumulator, a second reset means for the most significant bit of the second accumulator, and a third AND-means, where the output of said third AND-means is connected to said first and said second reset means of said first and said second accumulator, where the most significant bit of said first accumulator is connected to a first non-inverting input of said third AND-means, and where the

most significant bit of said second accumulator is connected to a second non-inverting input of said third AND-means.

9. A phase-locked loop according to claim 8, wherein the phase comparator includes a converter circuit having:

means for performing a first logic bit by bit AND operation of the output of the first accumulator and the inverted output of the second accumulator, and for generating a first analogue representation of said first logic bit by bit AND operation, and

means for performing a second logic bit by bit AND operation of the output of the second accumulator and the inverted output of the first accumulator, and for generating a second analogue representation of said second logic bit by bit AND operation.

10. A phase-locked loop according to claim 9, wherein the converter circuit comprises current mode logic circuits giving a current output for a two input AND operation, said current output being used for generating an analogue representation for a bit by bit AND operation.

11. A phase-locked loop according to claim 9 or 10, wherein the arithmetic means are adapted to obtain one or more analogue phase error signals based on the second analogue representation of the second logic bit by bit AND operation and the first analogue representation of the first logic bit by bit AND operation.

12. A phase-locked loop according to claim 11, wherein the arithmetic means comprises subtraction means being adapted for performing an analogue subtraction of the second analogue representation from the first analogue representation.

13. A phase-locked loop according to any one of the claims 8-12, further comprising a divider for dividing the frequency of the output signal, whereby the received output signal received by the phase comparator is a frequency-divided output signal.

14. A phase comparator for carrying out the method in accordance to claim 1-7, wherein the first signal is a reference signal and the second signal is an input signal, said phase comparator including:

a first accumulator adapted to add a first predefined phase step value to a first accumulated phase value in response to a reoccurring event in said reference signal,

a second accumulator adapted to add a second predefined phase step value to a second accumulated phase value in response to a reoccurring event in said input signal, and

means or arithmetic means for determining the phase error based on the second accumulated phase value and the first accumulated phase value,

said phase comparator further including a first reset means for the most significant bit of the first accumulator, a second reset means for the most significant bit of the second accumulator and a third AND-means, where the output of said third AND-means is connected to said first and said second reset means of said first and said second accumulator, where the most significant bit of said first accumulator is connected to a first non-inverting input of said third AND-means, and where the most significant bit of said second accumulator is connected to a second non-inverting input of said third AND-means.

15. A phase comparator according to claim 14, wherein the phase comparator includes a converter circuit having:

means for performing a first logic bit by bit AND operation of the output of the first accumulator and the inverted output of the second accumulator, and for generating a first analogue representation of said first logic bit by bit AND operation, and

means for performing a second logic bit by bit AND operation of the output of the second accumulator and the inverted output of the first accumulator, and for generating a second analogue representation of said second logic bit by bit AND operation.

16. A phase comparator according to claim 15, wherein the converter circuit comprises current mode logic circuits giving a current output for a two bit AND operation, said current output being used for generating an analogue representation for a bit by bit AND operation.

17. A phase comparator according to claim 15 or 16, wherein the arithmetic means are adapted to obtain one or more analogue phase error signals based on

the second analogue representation of the second logic bit by bit AND operation and the first analogue representation of the first logic bit by bit AND operation.

18. A phase comparator according to claim 17, wherein the arithmetic means comprises subtraction means being adapted for performing an analogue subtraction of the second analogue representation from the first analogue representation.